Yield*

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Abstract

This document covers yield of integrated circuit production.

Perhaps a word about feature size, chip size and yield would be in order. We saw earlier that circuits are repeated many times across a wafer's surface during the photolithographic stage. Although great care is exercised in trying to prevent defects from becoming part of a wafer surface (clean rooms, "bunny" suits, ultra-pure chemicals etc.) each wafer that goes through a fab will end up with **some** "killer" defects distributed across the wafer surface Figure 1 (A Wafer with Defects).

A Wafer with Defects

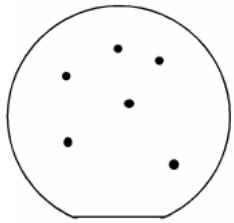

Figure 1

Imagine that we try to manufacture some chips of a certain size. A glance at Figure 2 (Six Killed Circuits) shows that we would have 15 of 21 good chips, for a yield of about 71%. Suppose we could, through improved technology, perform a 30% "shrink" on the circuit - *i.e.* make its dimensions 30% smaller. Now, as Figure 3 (Lots More Good Ones) shows, we get 40 good chips/wafer instead of 15 (and they cost no more to produce) and our yield has gone to 40 out of 46 or 87%. We will be rich! Or at least we won't go out of business!

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Six Killed Circuits

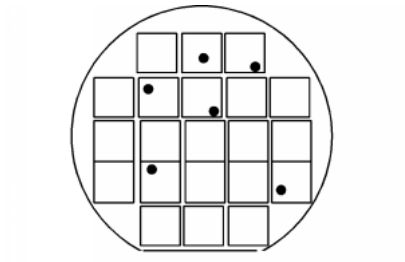

Figure 2

Lots More Good Ones

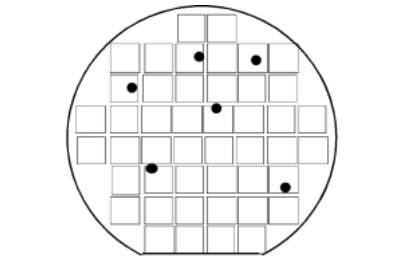

Figure 3

Yield, reliability and manufacturability are all critical issues in the semiconductor industry. The business is highly competitive, and the technology keeps moving rapidly. It is an exciting and challenging field, one which demands the very best, but which rewards someone who is willing to never stop thinking and to bring forth the very best creative solutions to hard problems.