

# FIR FILTERING: BASIC ASSEMBLY EXERCISE FOR TI TMS320C54X (中文版 CHINESE VERSION)\*

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Based on *FIR Filtering: Basic Assembly Exercise for TI TMS320C54x*<sup>†</sup> by

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### Abstract

You will work through a section of TI TMS320C54x assembly code by hand. The instructions include multiplication of fractional numbers in two's complement representation.

#### 1 [U+6C47] [U+7F16] [U+7EC3] [U+4E60]

分析下面的程序代[U+7801]。可以参考 Two's Complement and Fractional Arithmetic for 16-bit Processors<sup>1</sup>、Addressing Modes for TI TMS320C54x<sup>2</sup>、以及 *Mnemonic Instruction Set*[?] 等手册中的内容。

```

1  FIR_len .set    3
2
3  ; Assume:
4  ;   BK = 3
5  ;   ARO = 1
6  ;   AR2 = 1000h
7  ;   AR3 = 1004h
8  ;
9  ;   FRCT = 1
10
11     stl     A,*AR3+%
12     rptz   A,(FIR_len-1)
13     mac    *AR2+0%,*AR3+0%,A

```

任何以";" [U+5F00] [U+5934]的代[U+7801]行均[U+4E3A]注[U+91CA]。在[U+8FD9]里,注[U+91CA]行告[U+8BC9] [U+4F60]在第一"h" [U+7ED3]尾或以 0x [U+5F00] [U+5934]的数字均[U+4E3A] 十六[U+8FDB]制 数[U+503C]。

#### Example 1

1000h 和0x1000 均表示十[U+8FDB]制数[U+503C] 4096。

假[U+8BBE]起始地址[U+4E3A] 1000h的内存中的初始数据[U+4E3A]:

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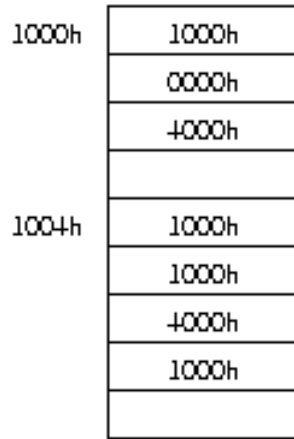
\*Version 1.7: Jul 18, 2004 1:37 am -0500

†<http://cnx.org/content/m10022/2.19/>

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<sup>1</sup>"Two's Complement and Fractional Arithmetic for 16-bit Processors" <<http://cnx.org/content/m10808/latest/>>

<sup>2</sup>"Addressing Modes for TI TMS320C54x" <<http://cnx.org/content/m10806/latest/>>



**Figure 1:** 内存中的数据分配([U+6267]行前)

在熟悉了 `stl`、`rptz` 和 `mac` 等指令后,逐行 [U+6267] 行代 [U+7801] 并将累加器 A 及 [U+8F85] 助寄存器 AR2 和 AR3 中的数 [U+503C] [U+8BB0] [U+5F55] 在 Figure 2 所提供的表格中。[U+53E6] 外,在三行指令全部 [U+8FD0] 行之后将内存中的数 [U+53E6] 在 Figure 3 所提供的表格中。

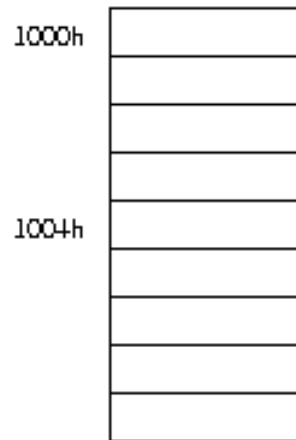
| A             | AR2   | AR3   |   |
|---------------|-------|-------|---|
| 00 0000 8000h | 1000h | 1004h | at start of code                          |
|               |       |       | after <code>stl</code> instruction        |
|               |       |       | after <code>rptz</code> instruction       |
|               |       |       | after first <code>mac</code> instruction  |
|               |       |       | after second <code>mac</code> instruction |
|               |       |       | after third <code>mac</code> instruction  |

**Figure 2:** [U+6267] 行 [U+7ED3] 果

在 [U+7EC3] [U+4E60] [U+8FC7] 程中要注意累加器 A 是40位寄存器,而且乘法器是工作在 分数算法模式 (**fractional arithmetic mode**) 下。在 [U+8FD9] [U+79CD] 模式下,所有 DSP 中的整数都被当作分数来 [U+5904] 理,ALU ([U+8FD0] 算器) 中整数乘法

Complement and Fractional Arithmetic for 16-bit Processors<sup>3</sup>中有更 [U+8BE6] [U+7EC6] 的描述。

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**Figure 3:** 内存中的数据分配 ([U+6267] 行前)

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<sup>3</sup>"Two's Complement and Fractional Arithmetic for 16-bit Processors" <<http://cnx.org/content/m10808/latest/>>