AE_Lecture8_MOSFET & JFET_PartA*

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Abstract

AE_Lecture8_PartA describes the structure and static characteristics of MOSFET.

AE_Lecture8_PartA Static characteristics of FIELD EFFECT TRANSISTORS

A Field Effect Transistor is like a pentode. It is an analogue of pentode. Both are Voltage Controlled Current Sources.

FET is of two types JFET and MOSFET.

JFET is n channel FET known as nJFET and p channel FET known as pJFET.

Similarly MOS is n channel NMOS and p channel PMOS.

MOS can be enhancement mode which is normally-off or depletion mode normally-on device.

So NMOS can be (E)NMOS and (D)NMOS.

PMOS can be (E)PMOS and (D)PMOS.

The following is the circuit diagram of an Amplifier using N-channel JFET:

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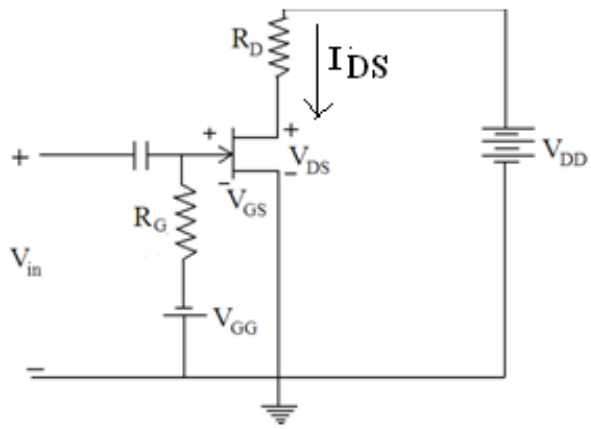

Figure 1. Circuit Set-up for measuring the Static Charactristics of nJFET.

Figure 1

Measurement of characteristics of N-channel JFET

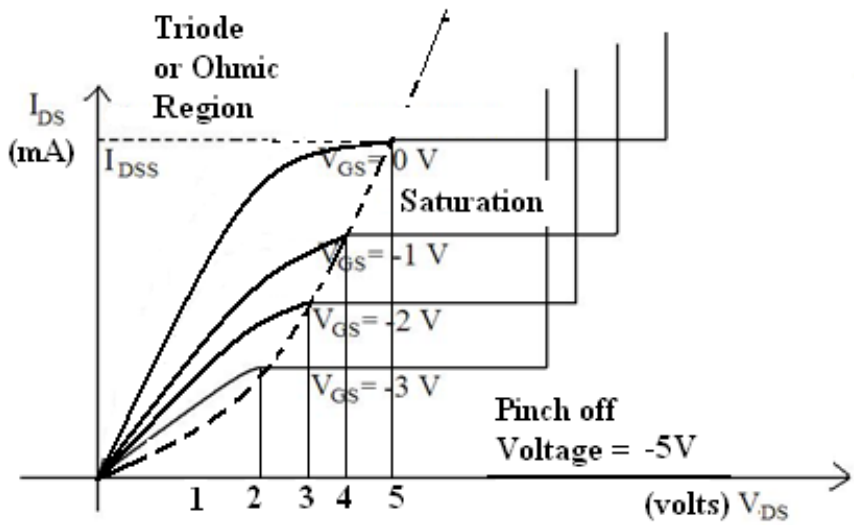

Figure 2. Static Output Characteristics of nJFET.

Figure 2

Figure 2 gives the dc output characteristics nJFET. Note that Gate Voltage is always kept negative so that the gate current is always zero. We indicate the Gate-Drain breakdown also. As gate voltage becomes more negative , Avalanche Breakdown of Gate to Drain Junction takes place earlier.When ($V_{DS} - V_{GS}$) exceeds V_P (Vpinchoff), the channel gets pinched off towards the Drain End and current becomes constant. This is saturation region. The dotted parabola seperates the Ohmic region or Triode Region from Saturation Region or Pentode Region. Here the pinch off voltage is -5V.

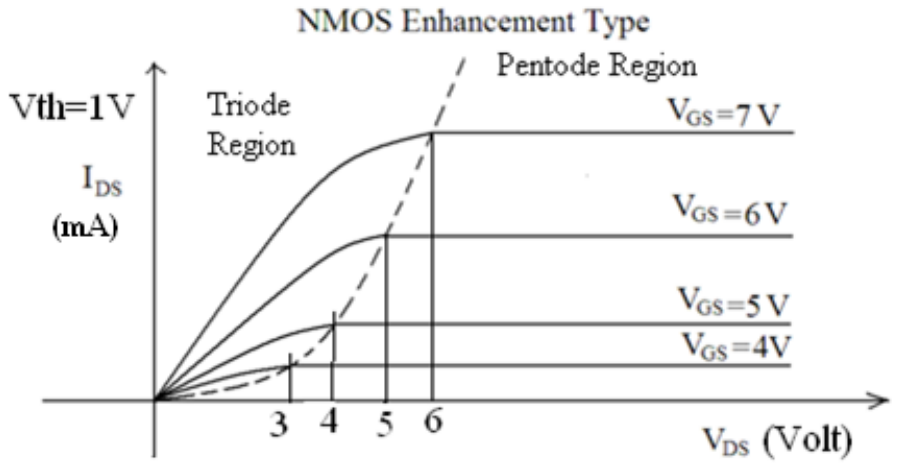

Figure 3. Static Output Characteristics of (E)NMOS.

Figure 3

Figure 3 gives the output characteristics of (E)NMOS with a Threshold Voltage of 1V. Therefore when V_{DS} increases and becomes equal to (V_{GS} - V_{Th}) the channel pinches off near the drain end and current saturates.. As V_{DS} assumes larger values the pinched off region becomes wider, (V_{GS} - V_{Th}) drops across the channel and excess part of V_{DS} drops across the pinched off region. Since there is a constant voltage dropping across the channel and since the channel is of constant length hence I_{DS} is constant. But in real life there is a shortening of channel length leading to a slope of the saturated current. This channel length modulation is responsible for a finite output impedance r_{ds} of the voltage controlled current source modeling (E)NMOS under incremental condition.

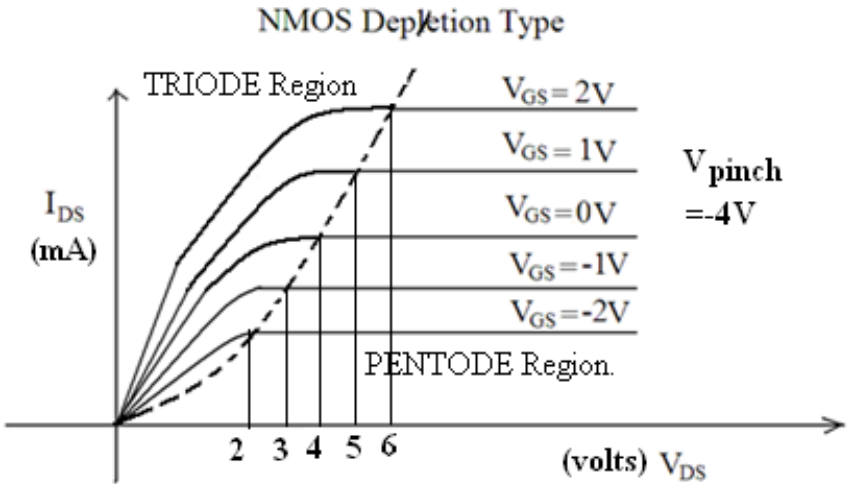

Figure 4.Static Output Characteristics of (D)NMOS.

Figure 4

In Figure 4 we give the output characteristics of (D)NMOS. Depletion type device is normally-on device hence it gives a characteristic for positive gate voltage, zero gate voltage and negative voltage. In (D)NMOS when gate voltage becomes equal to Pinch-off voltage then (D)NMOS turns off. Here pinch off voltage is -4V.

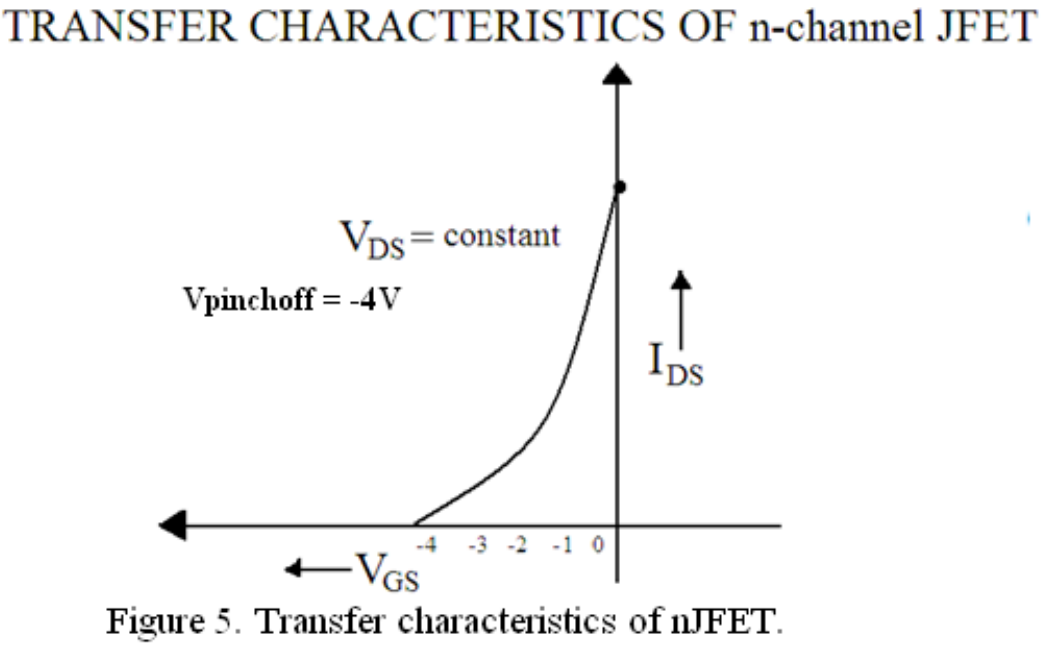
TRANSFER CHARACTERISTICS OF n-channel JFET
V_{DS} = constant
Vpinchoff = -4V
I_{DS}
-4 -3 -2 -1 0
V_{GS}
Figure 5. Transfer characteristics of nJFET.

Figure 5

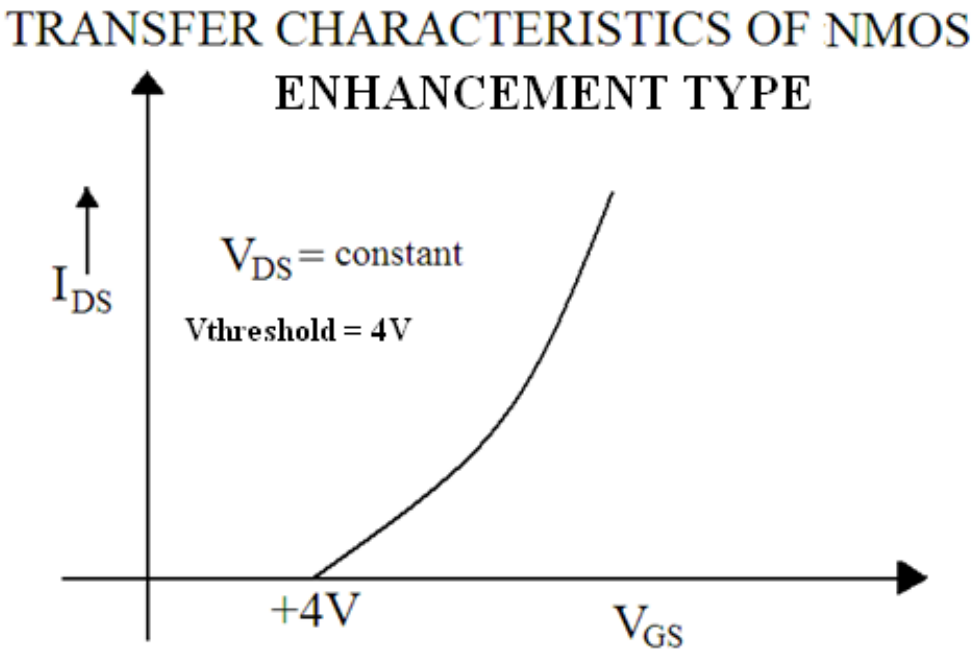

Figure 6. Transfer characteristics of (E)NMOS which is normally off device.

Figure 6

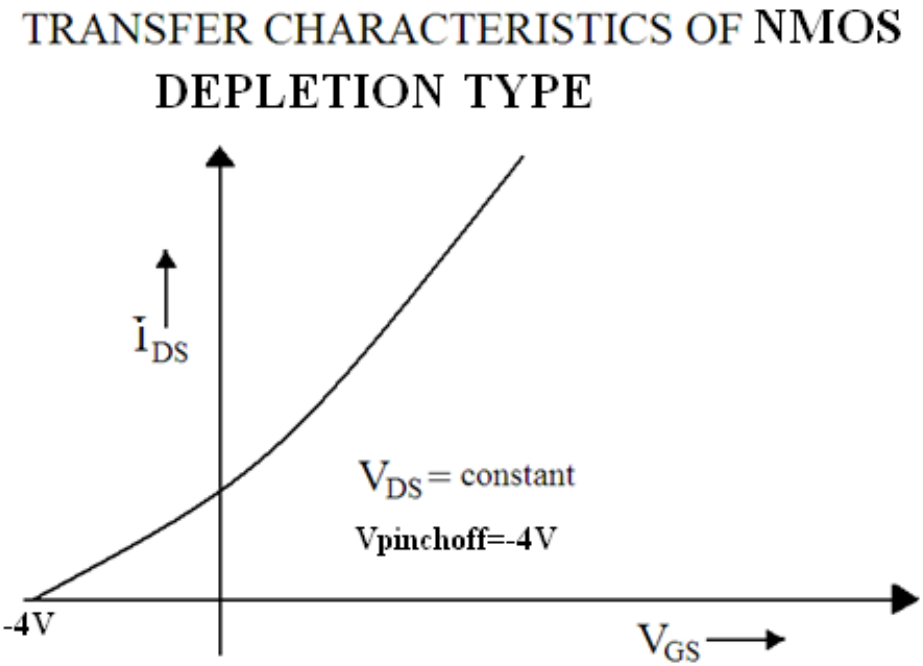

Figure 7. Transfer Characteristics of (D)NMOS which is normally on device.

Figure 7

Comparing the transfer characteristics of nJFET, (E)NMOS and (D)NMOS as given in Figure 5, 6 and 7 we can say that (D)NMOS is most flexible device from design point of view as it accepts both positive and negative voltages as the gate voltage.

NMOS Transistor (Pentode and Triode Region)

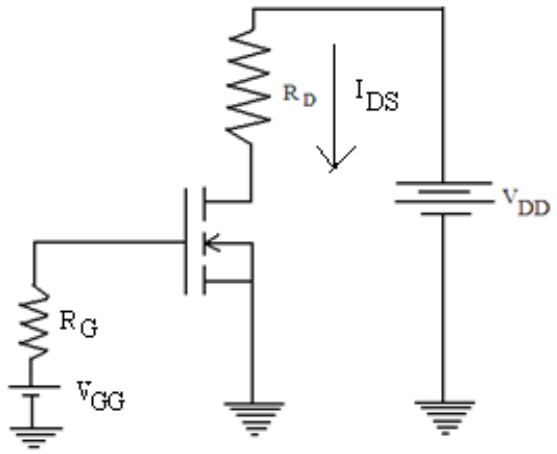

Figure 8. Circuit Set-up to study the Triode and Pentode Region of (E)NMOS.

Figure 8

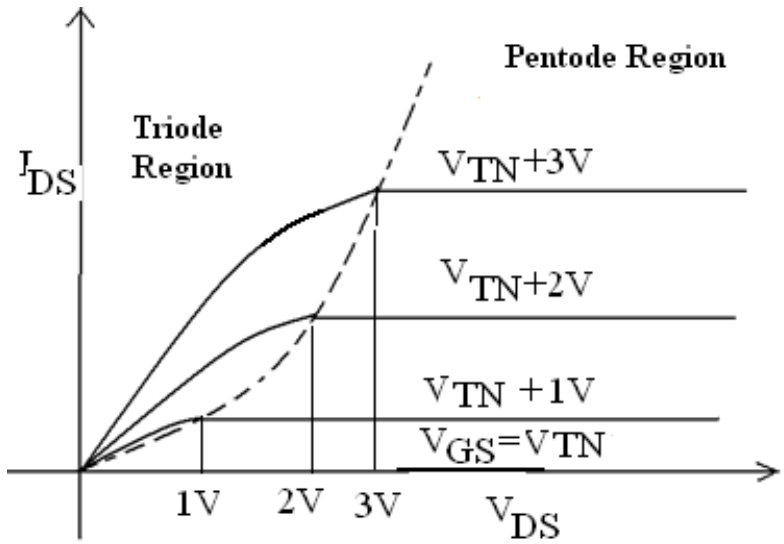

Figure 9. Output Characteristics of (E)NMOS demarcating the TRIODE and PENTODE region.

Figure 9

TRIODE REGION:

$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{(v_{DS})}{2}\right)(v_{DS})$$

Figure 10

_ _ _ _ _ _ (1)
K_n=K_n'multiplied_by

$$\left(\frac{W}{L}\right)$$

Figure 11

K_n'= $\mu_n C_{ox}''$ .....Kn' ia a transconductance parameter which is fixed for a given technology and cannot be changed by the circuit designer. Whereas Kn = Kn'×(W/L) = this is also a transconductance

parameter but it includes the aspect ration (W/L) of the given MOSFET. The aspect ratio gives the geometry of the device and this is under control of a circuit designer . This second transconductance parameter can be controlled when he is generating the masks for a given circuit or system during ASIC(Application Specefic IC) or SOC(System –on- Chip) design. W is the width of the gate and L is the length of the gate or the length of the channel.

$$\text{Cox}'' = \frac{\epsilon_{ox}}{T_{ox}}\left(\frac{F}{cm^2}\right)$$

Figure 12

$$\epsilon_{ox} = oxide\ permittivity\left(\frac{F}{cm}\right) = 3.9 \times 8.854 \times 10^{-14}\,\frac{F}{cm}$$

Figure 13

$$T_{ox} = oxide\ thickness$$

Figure 14

Triode Region exists as long as

$$(V_{GS} - V_{DS}) \geq V_{TN}$$

Figure 15

.
Channel should not pinch off on the drain side.
PENTODE REGION
At

$$V_{DS}^{*} = V_{GS} - V_{TN}$$

Figure 16

_____(2)
channel pinches off at drain end. From here onwards current becomes constant or current saturates. Substituting (2) in (1),

$$I_D = K_n \left(V_{GS} - V_{TN} - \frac{(V_{GS} - V_{TN})}{2} \right) (V_{GS} - V_{TN})$$

Figure 17

$$I_D = K_n \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 18

$$I_D = K_n^{\square} \frac{W}{L} \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 19

$$\therefore I_D = K_n^{\square} \frac{W}{L} (V_{GS} - V_{TN})^2$$

Figure 20

$$I_D = \mu_n C_{ox}'' \frac{W}{L} (V_{GS} - V_{TN})^2$$

Figure 21

Quadratic Law

$$I_D = \left[C_{ox}'' W \frac{(V_{GS} - V_{TN})}{2} \right] \left[\mu_n \frac{(V_{GS} - V_{TN})}{L} \right]$$

Figure 22

Where:

$C_{ox}'' W \frac{(V_{GS} - V_{TN})}{2}$ *is the average electron charge per unit length in the inversion layer*

Figure 23

And $\mu_n \frac{(V_{GS} - V_{TN})}{L}$ *is the drift velocity in the channel*

Figure 24

Pinch Off locus is parabolic

$$\because I_D = \frac{K_n (V_{DS}^*)^2}{2}$$

Figure 25

For any V_{GS} , at $V^*_{DS} = V_{GS} - V_{TN}$ the saturation sets in as the channel gets pinched off at that point. Beyond that point: $V_{DS} = V^*_{DS} + \Delta V$ and V^*_{DS} drops across the channel and ΔV drops across the depleted region towards the drain end as shown in Figure 11. Since the voltage across the channel is constant at V^*_{DS} and since the channel is approximately constant (it shortens slightly as Drain to Source Voltage increases) for practical purposes we assume that the drain current is constant and hence it has saturated. But in practice due to channel length shortening, there is slight increase in drain current with drain to source voltage. Hence output characteristics does have a slope. At higher currents the slope is higher.

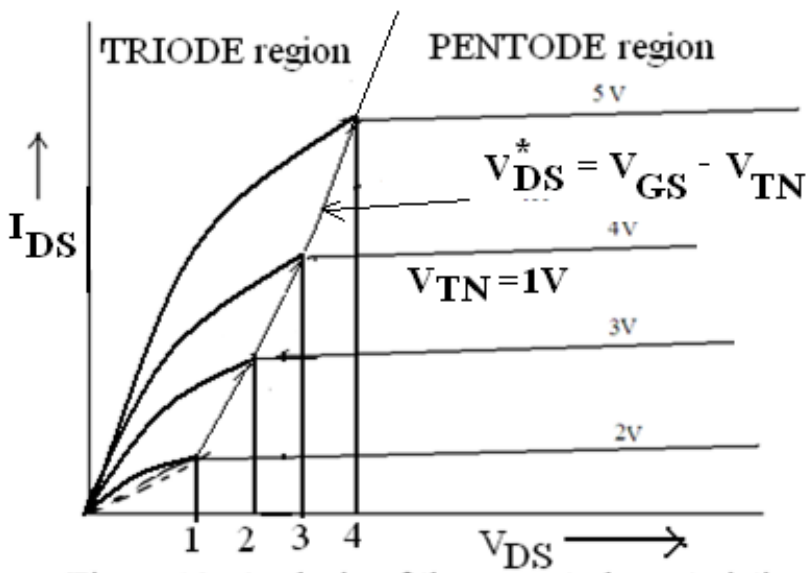

Figure 10. Analysis of the output characteristics of (E)NMOS for demarcating the TRIODE and PENTODE regions.

Figure 26

V_{TN}=1V
K_n=25 μA/V^2

$$i_D = K_n \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 27

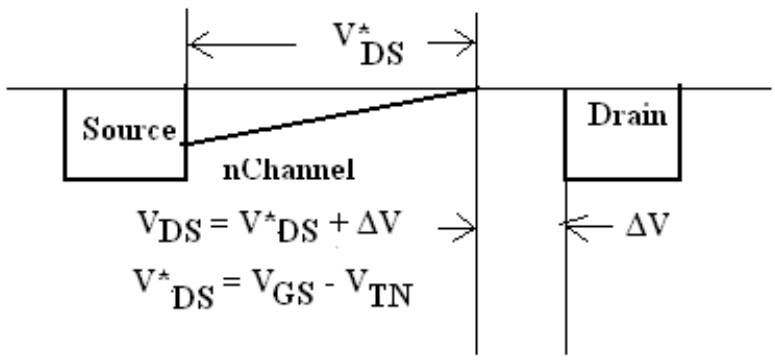

Figure 11. Physical mechanism of current saturation after the channel gets pinched off at drain end. Drain Current continues to flow evn though the channel is interrupted. At the drain end the electron manages to hop across the depletion region by Ballistic Mechanism.

Figure 28

N channel JET has identical formulation except threshold voltage is replaced by pinch off voltage.