Digital System Design Chapter 1 Part 2 Introduction to VLSI

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Abstract
DSD_Chapter 1_Part 2 introduces us to the EDA tools for implementing large and complex Digital Systems on IC chip at VLSI level.

Digital System Design Chapter 1 Part 2
Introduction to VLSI

Very Large Scale Integration:
It is the process of integrating millions of transistors on tiny silicon chips to perform a multitude of logic operations.

How do we design such complex VLSI Chips?
Programmable Logic Devices (PLDs) offer a practical way of implementing large and complex Digital Systems on IC chip.

When a particular Digital System is required in very large quantity it may become more economical to develop an optimized system dedicated to one particular application. IC chip implementation of such an optimized, dedicated PLD is called Application Specific Integrated Circuits (ASIC).

For design & development of PLDs and ASIC we have sophisticated Electronic Design Automation (EDA) tools.
EDA design tools have reasonably kept pace with designers need as shown in the following chart:

EDA design tools have gone from
Transistors

↓

Gate Level

↓

Register Transfer Level (RTL)

↓

Graphic Design System II (GDS II)

Classification of Programmable Logic Devices

*Version 1.3: Jul 27, 2010 11:00 am -0500
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Figure 12. Major Programmable Logic Devices.

ROM and MPGAs are programmed only once in the semiconductor fab itself whereas field programmable can be programmed and reprogrammed according to the need. ROM is thought to be a Memory Device but it can used as combinational circuit also as already seen in Digital Electronics Theory Classes. MPGAs are popular ways of achieving ASICs.

PLAs and PALs contain array of gates.

PLAs contain programmable AND array and programmable OR array. This allows users to implement combinational functions in two levels of gates.

In PAL, OR array is fixed and AND array is programmable. PALs also contain flip-flops.

Monolithic Memories Incorporation (MMI) and Advanced Micro Devices have developed a programming language which converts Boolean equations into PLA configurations.

Ultraviolet Erasures did not permit field programming. Only with the development of Electrically Erasable Technology that field programmable PLDs became technically feasible.

<table>
<thead>
<tr>
<th></th>
<th>SPLD</th>
<th>CPLD</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>Few hundred gates</td>
<td>500 to 12000 gates</td>
<td>3000 to 5M gates</td>
</tr>
<tr>
<td>Timing</td>
<td>predictable</td>
<td>predictable</td>
<td>unpredictable</td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Major Vendors</td>
<td>Lattice Sem.; Cypress; AMD;</td>
<td>Xilinx; Altera;</td>
<td>Xil; Alt; Lat. Sem; Actel;</td>
</tr>
<tr>
<td>Device families</td>
<td>L.S.GAL16LV8, GAL22V10;</td>
<td>Xil. cool runner, XC9500;</td>
<td>Xil. Virtex, Spartan;</td>
</tr>
</tbody>
</table>

Table 1: A comparison of Programmable Devices.

Table 5. A comparison of Programmable Devices

Electrically erasable CMOS PLD replaced PAL and PLA. PLDs contain macroblocks with array of gates, multiplexers, Flip Flops or other standard Building Blocks.

http://cnx.org/content/m34695/1.3/
Lattice Semiconductor created similar devices with easy programmability and called its line of devices generic array logic or GAL.

PLAs, FALs, GALs, PLDs and PROM are collectively called Simple Programmable Logic Devices or SPLD.

When multiple PLDs are put together in the same chip with crossbar interconnection and have the sizes of 500 to 16000 gates then we achieve Complex Programmable Logic Devices.

In 1980 Xilinx created FPGAs using Static RAM. This integrates a large number of logic. FPGAs donot have gate array but they have bigger and complex blocks of Static RAM and multiplexers.

Seeing the performance of Xilinx, several PLD vendors and Gate Array Companies jumped into the market. A variety of FPGA architecture were developed and used. Some are reprogrammable and some are one-time programmable fuse technologies. In last 15 years FPGAs have grown up to a size of 5 million gates.

**Why VLSI ?**

- Building complex electronic circuit using discrete components are difficult and expensive - Cost depends on quantity of devices.
- Integrated circuits solved much of the problems

- Print many tiny circuits on a flat surface – "easy" as taking pictures.
- Cost depends on die size.

- CPLD stands for Complex Programmable Logic Device, Advanced version of PLD's.

Here new resources are available such as Flip-Flops, Gates in high number and are able to give functionality of circuits consisting of few thousand gates and few hundred flip-flops.

- FPGA (Field Programmable Gate Arrays) is another programmable resource having very higher programmability than CPLD.
- Then there are other higher technology resources (ASIC’s) which can be used to design many complex circuit like microprocessors or bus controllers.
- Applications requiring user defined functions like bit processing or DSP algorithm combined with other computational capabilities.
- Thus you are actually designing for emerging and complex Technologies.

**VLSI Advantages**

1. Reduction in size, power, design, cycle time.
2. Design security.
3. Easy up-gradation.
4. Low cost.
5. Remote Programmability.

**VLSI Techniques**

- VLSI stands for Very Large Scale Integration. This is the technology of putting millions of transistors into one silicon chip.
- Tools (for VLSI):

  A. Modelsim 6.2G: Simulation

Simulation is used for testing the behavior of outputs on the waveform according to their input given.
A. Leonardo Spectrum 3: Synthesis

Synthesis tool is used for looking the hardware according to the program written in their language like, VHDL/VERILOG.

A. Xilinx 10.1 ISE Pack: Chip downloading

Evolution of programmable Devices:

1) PROM: Programmable ROM
2) PAL: Programmable Array Logic.
3) PLA: Programmable Logic Array.
4) CPLD: Complex Programmable Logic Devices.
5) FPGA: Field Programmable Gate Arrays.
6) ASIC: Application Specific ICs.

PLD Trend

Figure 2

Figure 13. Volume of Application versus the building block

New FPGA Revolution:

1) All disadvantages of ASICs have been overcome by FPGA namely:
   a. Longer time to market.
   b. Complex Design Methodology.
2) In terms of No. of Transistors per chip, FPGA Vendors have increased its capacity and astounding results are achieved as time pass through.
3) Inclination towards FPGA is increasing day by day.
4) Leverage existing design / chipset to support multiple display types.
5) Faster time to market.
6) Improve inventory control.
7) Customize products for different geographies.
8) Reduce exposure to supply issues
   - a. Flexibility to efficiently manage component supply problems.
9) Reacts quickly to competitive pressures

- Bringing new features / capabilities rapidly to market.

**FPGA Price Revolution:**

![Figure 3: Price of 100 K gates over time.](http://cnx.org/content/m34695/1.3/)

Cost Management through System Integration:
Figure 4

- Replacing discrete parts
  - Dual port memory FIFO
  - Clock buffers
  - Localized clock drivers
  - DLLs
  - Level translators
  - Hot socketing
  - Schmitt triggers
  - TTL devices
  - Backplane drivers
  - Board deskew

- Benefits
  - Cost savings
  - Fewer components
  - Board area savings
  - Higher reliability

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Figure 15. Cost management through System Integration.

Embedded Advantage

- Complete System Design Possible.
- Real Time Application.
- Low Cost Chip.
- VLSI goes on embedded as we can write program in Linux and Unix Environment.
- System C developed by Xilinx.

Chip Design application Areas:

- VLSI in Wireless Communication
- Digital Imaging
- DSP Design
- High Level synthesis
- Logic Design
- ASIC Design
- Processor Design
- Low Power Design
- Issues in deep-sub micron VLSI
- Electronic Design Automation (EDA) tools
- Mixed Signal Design
- All aspects of test and DFT
- Most systems are now FPGA/ASIC based
• Networking (PCI, Ethernet USB)
• DSP & Communication
• Speech & Image Processing
• Tele Mobile Communication
• Microprocessor & Microcontroller based System
• Home Appliances
• Real Time Applications

Latest Chip Design Trend

• Auto Motive Sector
• Biometric analysis for security
• Neural Network & Artificial Intelligence
• System on chip design with virtual component
• Bio-chips: Rule Based System
• Neuro Chips

FABRICATION PROSPECT:

1. Chip Design Productivity
2. Chip Design Forecast
3. World Fab Industry Vs Indian Fab Industry
4. Why Fab lab does not exist in India?
5. Challenges before Chip Design and Fab lab

Chip Design Productivity

Figure 5

Figure 16. Actual No. of Transistors in millions per IC design. This data illustrates that there is little correlation between transistors count and engineering effort.

http://cnx.org/content/m34695/1.3/
Figure 6

Figure 17. Normalized Transistor Count Vs. Persons week.

Figure 7

Figure 18: Factors Influencing IC Design Effort
Design Productivity = output produced / labour expended
= output per unit worker hour

Manufacturing productivity = value added / labour expended
= value added per unit worker hour.
= (end product selling price - material cost of the product) worker hour
= dollars per worker hour

Chip design productivity = transistor / gate per unit engineering effort.

Chip design productivity = chip design complexity / engineering effort.
= complexity per unit engineering hour.
= normalized transistors per person-hour.

Chip Design Forecast:
According to Indian Semiconductor Association (ISA) quoting the ISA-IDC Report of 2008, by that year the Semiconductor activity in India had a turnover of $7.37 billion employing over 150,000 highly qualified professionals. Embedded Software Design constituted a whopping 81% of this activity with VLSI design being 13% and hardware / board design being 6%. The growth rate of this sector is some 20% annually, so we can expect a turnover in excess of $12 billion by the end of Year 2010 (employing 180,000+ professionals) of which embedded system design would have a turnover of 10 billion. It is believed that the global embedded design activity is worth some $25 billion annually. This roughly amounts to India producing a quarter of the world’s embedded design systems. The growth in the design business to the rapid growth of the Indian Electronics Industry from $363 billion by 2015 at a compounded annual growth rate of some 30%, accounting for 11% of the global market by 2015, projected to grow to $155 billion by 2015.

World Fab Industry Vs Indian Fab Industry:

a. Around 50 Fab lab exist in the world, another 50 in near future.
b. First Fab lab by Intel just open in Tiw an, first in South Asia.
c. No complete VLSI Fab lab in India.
d. SCL, Chandigarh has its own LSI fab lab.
e. Proposal: Rs.1500 crore (for Indian Govt.).
f. Recently, three companies joined forces in Fab industry like: Sem India, HEMC, and Alliance Materials.

Fab lab does not exist in India: Why?

1. Huge fabrication Lab Cost:
As fabrication unit requires minimum 1500 crore rupees investment, it’s not feasible for many small Indian companies to make sustained investments for a long period of time, which is required for product development (including the area of chips design / manufacturing).

2. Design In competency, Probably India is not prepared:
The actual problem is that quality talent with the right skills is becoming scarce. The skills required are in vertical domains (DSP, TELECOM, etc.) along with in depth understanding of chip design challenges like designing for high speed, low power, small size, handling large complexities, accounting for deep sub-micron effects like signal integrity.

Challenges before Chip Design and Fab Industry:

1. System Level Integration: there is requirement of system engineers who can understand the complete system. The trend towards coding is to write code in C/C++, Matlab / Java and converted into HDL / VERILOG, is not suitable.

2. Chip Design Limits: Chip Design, reported by New York Times by at Paul Packan, a scientist with Intel Corp., the world largest chipmaker, said semiconductor engineers have not found ways around basic physical limits beyond the generation of silicon chips that will begin to appear next year. Packan called the apparent impasse “the most difficult changes the semiconductor industry has ever faced.”

http://cnx.org/content/m34695/1.3/
These fundamental issues have not previously limited the scaling of transistors,” Packan wrote in the Sept.
24 issue of Science. “There are currently no known solutions to these problems.”

According to Dennis Allison, a Silicon Valley physicist and computer designer, if the miniaturization
process for silicon based transistors is halted, hopes for continued progress would have to be based on new
materials, new transistor designs and advances like molecular
computing, the Times reported. This mystery will be solved ultimately.

Can we meet the challenges of the Future?
[“Can you meet the design challenges of 90nm and below?”, Electronic Design, 2005]
[“Nano-computers”, by Phillips J. Kurkes, Gregory S. Snider & R.Stanley William, Scientific American,
November 2005, 72-80.]

Unprecedented manufacturing success has been achieved by enhancing the ability of number crunching,
executing enhanced FLOPS(floating point operations per second)/Instructions per second and by enhanced
data storage capability.

Historically we have moved from labour intensive techniques to capital intensive techniques. Presently
we are witnessing a movement towards knowledge intensive techniques.

Agricultural labour were replaced by proletariate(industrial labour) and proletariate are being replaced
by cognetariate(knowledge worker).

Introduction of computerization, automation and robotization has changed the benchmarks of life.

Silicon Industry has become the largest and most influential industry.

Major innovation will be required to reach 10nm feature size. Finding alternative technologies that can
further shrink computing devices is crucial to maintaining technological progress. Alternative technology
could be ‘Quantum Computing’ and ‘Cross-Bar Architecture’.

In Cross-Bar Architecture, one set of nano-wires cross another set of nano-wires at right angles. A special
material is sandwiched at the intersection between the crossing wires. This sandwiched material could switch
on and off. Logic functions as well as memory functions could be achieved using the intersections.

As the packing density increases, atomic defects become a serious problem. This problem could be
circumvented by building redundancy and by using coding technique. By using Error Correcting Codes the
error rates at the intersection could be drastically reduced. By introducing 40% redundancy the yield of
manufacturing could improve from 0.0001 to 0.9999 if the defect rate is 0.01.

Today Cross Bar Architecture has emerged as the principal contender for a new computing paradigm.
For this success, architecture, device physics and nano-manufacturing techniques need to simultaneously
develop.

Cross Bare Architecture is ideal for implementing strategies based on finding and avoiding defect areas
and using coding theory to compensate for mistakes.

Such switches should be able to scale down to single atom dimension.